UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,971	03/10/2004	Te-Haw Lee	1007-043	6255

22898 7590 07/07/2005

THE LAW OFFICES OF MIKIO ISHIMARU
1110 SUNNYVALE-SARATOGA ROAD
SUITE A1
SUNNYVALE, CA 94087

EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/797,971	LEE ET AL.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, as disclosed in figures 1A-1B, and their description on pages 1-2 of the instant application, in view of Ikenaga et al. (U.S. Patent No. 6,744,118) and further in view of Fan et al. (U.S. Patent No. 6,400,004). With regard to Claim 1, Applicant's admitted prior art discloses a surface-mount enhanced lead-frame, comprising:

a die pad (11);

a plurality of leads (12) disposed around the die pad (figure 1A).

Applicant's admitted prior art fails to disclose a dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad and a solder metal layer formed on a surface of the indentation of the dam bar structure of the lead frame

However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having leads (L). Therefore, it would have been obvious to someone with ordinary skill in the art, at the

time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

Regarding the claimed solder metal layer formed on a surface of the indentation of the dam bar structure of the lead frame, Fan discloses a leadless semiconductor package which includes a die pad (330), leads (340), the leads are half-etched to form an indentation (340a) (column 4, lines 39-43) and are part of a lead frame made from a metal strip, wherein a metal flash comprising nickel, palladium and gold is formed on said metal strip (column 5, lines 6-12). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed solder metal layer formed on a surface of the indentation of the dam bar structure of the lead frame, as suggested by Fan, in order to prevent corrosion and contamination to the die pad and the leads (column 5, lines 10-12).

With regard to Claim 2, Applicant's admitted prior art discloses a lead-frame that is a quad-flat non-leaded (QFN) lead-frame (page 1, lines 23-25 of the instant application)

With regard to Claim 3, a further difference between the claimed invention and Applicant's admitted prior art is, the claimed indentation formed by chemical-etching or punching method.

However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having leads (L), wherein the groove portions are done by etching (column 3, lines 22-23). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed the claimed indentation formed by chemical-etching or punching method, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

With regard to Claim 4, Applicant's admitted prior art discloses (page 2, lines 13-18 of the instant application) a solder metal layer (16) formed on the surface of the lead frame (10).

Applicant's admitted prior art fails to disclose the claimed indentation in a dam bar structure. However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having leads (L). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

With regard to Claim 5, Applicant's admitted prior art discloses (page 2, lines 13-15 of the instant application) a solder metal layer (16) made of metal palladium (Pd) and that is pre-plated on a surface of a lead-frame (10).

With regard to Claim 6, Applicant's admitted prior art discloses (page 2, lines 13-18 of the instant application) a solder metal layer (16) made of tin/lead (Sn/Pb) covering an exposed surface of a lead-frame (10) after a molding process is conducted to form a package-body coupled to the lead-frame. It is further noted that the limitation "after a molding process is conducted to form a package-body coupled to the lead-frame" is a product-by-process that does not structurally or patentably distinguish the claimed invention from the structure disclosed by Applicant's admitted prior art. The method of forming a device is not germane to the issue of patentability of the device itself.

With regard to Claim 7, Applicant's admitted prior art discloses a surface-mount enhanced lead-frame, comprising:

a lead-frame (10) comprising a die-pad (11) and a plurality of leads (12) disposed around the die pad (figure 1A),

at least a semiconductor chip (13) bonded on the die pad (figure 1A), and electrically connected through wires (14) to the leads; and

a package body (15) formed to encapsulate the semiconductor chip and the lead frame.

Applicant's admitted prior art fails to disclose a dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad and a solder metal layer formed on a surface of the indentation of the dam bar structure of the lead frame

However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having leads (L). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

Regarding the claimed solder metal layer formed on a surface of the indentation of the dam bar structure of the lead frame, Fan discloses a leadless semiconductor package which includes a die pad (330), leads (340), the leads are half-etched to form an indentation (340a) (column 4, lines 39-43) and are part of a lead frame made from a metal strip, wherein a metal flash comprising nickel, palladium and gold is formed on said metal strip (column 5, lines 6-12). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed solder metal layer formed on a surface of the indentation of the dam bar structure of the lead

frame, as suggested by Fan, in order to prevent corrosion and contamination to the die pad and the leads (column 5, lines 10-12).

With regard to Claim 8, Applicant's admitted prior art discloses a lead-frame that is a quad-flat non-leaded (QFN) lead-frame (page 1, lines 23-25 of the instant application)
With regard to Claim 9, a further difference between the claimed invention and Applicant's admitted prior art is, the claimed indentation formed by chemical-etching or punching method. However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having leads (L), wherein the groove portions are done by etching (column 3, lines 22-23). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed the claimed indentation formed by chemical-etching or punching method, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

With regard to Claim 10, Applicant's admitted prior art discloses (page 2, lines 13-18 of the instant application) a solder metal layer (16) formed on the surface of the lead frame (10).

Applicant's admitted prior art fails to disclose the claimed indentation in a dam bar structure. However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having

leads (L). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

With regard to Claim 11, Applicant's admitted prior art discloses (page 2, lines 13-15 of the instant application) a solder metal layer (16) made of metal palladium (Pd) and that is pre-plated on a surface of a lead-frame (10).

With regard to Claim 12, Applicant's admitted prior art discloses (page 2, lines 13-18 of the instant application) a solder metal layer (16) made of tin/lead (Sn/Pb) covering an exposed surface of a lead-frame (10) after a molding process is conducted to form a package-body coupled to the lead-frame. It is further noted that the limitation "after a molding process is conducted to form a package-body coupled to the lead-frame" is a product-by-process that does not structurally or patentably distinguish the claimed invention from the structure disclosed by Applicant's admitted prior art. The method of forming a device is not germane to the issue of patentability of the device itself.

With regard to Claim 13, Applicant's admitted prior art discloses a method for fabricating a semiconductor package with a surface-mount-enhanced lead-frame, comprising:

preparing a lead frame module plate (page 2, lines 7-10 of the instant application) which consists of a plurality of lead frames (10) arranged in matrix form (page 2, line 10 of the instant application) wherein any two of the neighboring lead frames are separated by a bar structure, and wherein the lead-frame comprises a die-pad (11) and plurality of leads (12) disposed around the die-pad in a manner that ends of the leads oriented away fro the die pad are connected to the dam bar structure;

bonding at least semiconductor chip (13) on the die-pad of each of the lead-frame;

electrically connecting through wires (14) the semiconductor chip to the corresponding leads;

forming a package body (15) on the lead-frame module plate to cover the lead frames and the semiconductor chips.

Applicant's admitted prior art fails to disclose the steps of providing a dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad and performing a singulation-process along the indentations of the dam bar structures so as to separate the lead frame module plate mounted with the semiconductor chips and package body into a plurality of semiconductor packages and a solder metal layer formed on a surface of the indentation of the dam bar structure of the lead frame

However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having

leads (L) and performing a singulation-process along the indentations of the dam bar structures so as to separate the lead frame module plate mounted with the semiconductor chips and package body into a plurality of semiconductor packages (column 2, lines 36-49).

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the method as disclosed by Applicant's admitted prior art to include the claimed steps of providing a dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad and performing a singulation-process along the indentations of the dam bar structures so as to separate the lead frame module plate mounted with the semiconductor chips and package body into a plurality of semiconductor packages, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

Regarding the claimed solder metal layer formed on a surface of the indentation of the dam bar structure of the lead frame, Fan discloses a leadless semiconductor package which includes a die pad (330), leads (340), the leads are half-etched to form an indentation (340a) (column 4, lines 39-43) and are part of a lead frame made from a metal strip, wherein a metal flash comprising nickel, palladium and gold is formed on said metal strip (column 5, lines 6-12). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed solder metal layer formed on a surface of the indentation of the dam bar structure of the lead

frame, as suggested by Fan, in order to prevent corrosion and contamination to the die pad and the leads (column 5, lines 10-12).

With regard to Claim 14, Applicant's admitted prior art discloses a lead-frame that is a quad-flat non-leaded (QFN) lead-frame (page 1, lines 23-25 of the instant application)

With regard to Claim 15, a further difference between the claimed invention and Applicant's admitted prior art is, the claimed indentation formed by chemical-etching or punching method. However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having leads (L), wherein the groove portions are done by etching (column 3, lines 22-23). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed the claimed indentation formed by chemical-etching or punching method, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

With regard to Claim 16, Applicant's admitted prior art discloses (page 2, lines 13-18 of the instant application) a solder metal layer (16) formed on the surface of the lead frame (10).

Applicant's admitted prior art fails to disclose the claimed indentation in a dam bar structure.

However, Ikenaga discloses frame for a semiconductor package which includes a metal frame having groove portions (12) which pass through areas of a lead-frame corresponding having leads (L). Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed dam bar structure formed with an indentation that is integrally formed to be connected to each end of the leads away from the die pad, as suggested by Ikenaga, in order to decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

With regard to Claim 17, Applicant's admitted prior art discloses (page 2, lines 13-15 of the instant application) a solder metal layer (16) made of metal palladium (Pd) and that is pre-plated on a surface of a lead-frame (10).

With regard to Claim 18, Applicant's admitted prior art discloses (page 2, lines 13-18 of the instant application) a solder metal layer (16) made of tin/lead (Sn/Pb) covering an exposed surface of a lead-frame (10) after a molding process is conducted to form a package-body coupled to the lead-frame. It is further noted that the limitation "after a molding process is conducted to form a package-body coupled to the lead-frame" is a product-by-process that does not structurally or patentably distinguish the claimed invention from the structure disclosed by Applicant's admitted prior art. The method of forming a device is not germane to the issue of patentability of the device itself.

With regard to Claims 19 and 20, a further difference between the claimed process and Applicant's admitted prior art is, the singulation-process being a punching-process and using a branched-punching cutting tool. However, Ikenaga discloses a singulation-process using a cutting tool (dicing saw), which can be used in a punching-process. Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Applicant's admitted prior art to include the claimed the singulation-process being a punching-process and using a branched-punching cutting tool, as suggested by Ikenaga, in order to inhibit generation of metal-dust (column 2, lines 28-35) and decrease the generation of burrs during a dicing process and prevent short-circuiting (column 4, lines 12-20).

Response to Arguments

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

E.O.
A.U. 2815
7/1/05

JEROME JACKSON
PRIMARY EXAMINER